CLAIMS

What is claimed is:

1. A power estimation system, comprising:

area data associated with transistor gate area of at least one unit of a circuit design; and

a power estimation engine that determines a relative estimation of power for the at least one unit of the circuit design based on a predetermined correlation that characterizes device power as a function of transistor gate area.

2. The system of claim 1, the power estimation engine determines the relative estimation of power by employing at least one coefficient that characterizes device power as a function of transistor gate area.

3. The system of claim 2, the at least one coefficient defining a substantially linear relationship between device power and transistor gate area, such that the at least one coefficient includes a multiplier coefficient and an offset coefficient.

4. The system of claim 1, the relative estimation of power is based on a determination of static power and dynamic power.

5. The system of claim 4, the relative estimation of power is also based on a determination of gate leakage power.

6. The system of claim 1, the area data comprising high voltage threshold (HVT) transistor gate area data and low voltage threshold (LVT) transistor gate area data.

7. The system of claim 6, the power estimation engine employs a first predetermined correlation of power based on HVT transistor gate area data that characterizes HVT device power as a function of HVT transistor gate area and a second predetermined correlation of power based on LVT transistor gate area that characterizes LVT device power as a function of LVT transistor gate area.

8. The system of claim 7, the first predetermined correlation being a first set of at least one coefficient that characterizes HVT device power as a function of HVT transistor gate area and the second predetermined correlation being a second set of at least one coefficient that characterizes LVT device power as a function of LVT transistor gate area, the relative estimation of power for the at least one unit of the circuit design is computed by adding the power determined for the HVT devices and the power determined for the LVT devices.

9. The system of claim 8, the estimation of power for the at least one unit of the circuit design being further computed by adding a gate leakage power estimation based on both the HVT transistor gate area and the LVT transistor gate area and a third set of at least one coefficient based on a predetermined correlation that characterizes gate leakage power as a function of HVT transistor gate area and LVT transistor gate area.

10. The system of claim 1, further comprising an area calculator that generates the area data by analyzing a netlist provided by an optimization tool.

11. The system of claim 10, the area calculator and the power estimation engine cooperate with the optimization tool to generate a plurality of relative power estimates based on a plurality of circuit sizing instances of the at least one unit of the circuit design, the plurality of relative power estimates having a relative relationship to one another based on the predetermined correlation.

12. The system of claim 1, the correlation of power with respect to transistor gate area is determined by analyzing power data and associated transistor gate area data based on a plurality of instances of at least one circuit design type.

13. A system for determining an estimation of power for at least one unit of a circuit design, the system comprising:

a first power estimator that determines an estimation of relative power associated with high voltage threshold (HVT) devices by employing an HVT transistor gate area calculation and a predetermined functional relationship of HVT transistor gate area to HVT device power;

a second power estimator that determines an estimation of relative power associated with low voltage threshold (LVT) devices by employing an LVT transistor gate area calculation and a predetermined functional relationship of LVT transistor gate area to LVT device power; and

an adder that adds the relative estimation of powers from the first power estimator and the second power estimator to provide a total relative estimation of power.

14. The system of claim 13, further comprising a third power estimator that determines an estimation of relative power associated with LVT and HVT device gate leakage by employing the LVT transistor gate area calculation and the HVT transistor gate area calculation and a predetermined functional relationship of LVT and HVT transistor gate area to gate leakage power, the adder further adding the relative estimation of power from the third estimator to provide the total relative estimation of power

15. The system of claim 14, the relationship of HVT transistor gate area to HVT device power being a linear relationship and the relationship of LVT transistor gate area to LVT device power being a linear relationship.

16. The system of claim 14, the power estimate of the first power estimator comprising a HVT static power estimate and a HVT dynamic power estimate and the power estimate of the second power estimator comprising a LVT static power estimate and a LVT dynamic power estimate, the first power estimator and the second power estimator employ dynamic and static weight factors in determining the weight associated with the static and dynamic power estimates.

17. The system of claim 13, further comprising an area calculator that generates the LVT transistor gate area calculation and the HVT transistor gate area calculation by analyzing a netlist defining the at least one unit of a circuit design.

18. The system of claim 17, the area calculator analyzes netlists associated with circuit sizing instances of the at least one unit of the circuit design generated by an optimization tool.

19. A power estimator, comprising:

means for characterizing power as a function of circuit transistor gate area;

means for generating transistor gate area calculations for a plurality of circuit sizing instances associated with a circuit design; and

means for computing relative power estimates of the plurality of circuit sizing instances employing the transistor gate area calculations and the characterization of power as a function of circuit transistor gate area.

20. The power estimator of claim 19, the means for characterizing power as a function of circuit transistor gate area comprising a first characterizing of power as a function of high voltage threshold (HVT) transistor gate area, a second characterizing of power as a function of low voltage threshold (LVT) transistor gate area, and a third characterization of gate device leakage power based on LVT transistor gate area and HVT transistor gate area.

21. The power estimator of claim 20, the means for computing relative power estimates comprising computing relative power estimates associated with HVT transistor gate area, LVT transistor gate area and gate leakage transistor gate area.

22. The power estimator of claim 21, the means for computing relative power estimates computes relative power estimates for both static and dynamic power associated with both HVT devices and LVT devices.

23. A power estimation method for a circuit design, comprising:

calculating the transistor gate area associated with a circuit design; and

estimating relative power by computing a predetermined characterization of power as a function of transistor gate area.

24. The method of claim 23, the predetermined characterization of power as a function of transistor gate area being a substantially linear relationship that employs at least one of a multiplier coefficient and an offset coefficient to define power as a function of transistor gate area.

25. The method of claim 23, the estimating relative power by computing a predetermined characterization of power as a function of transistor gate area comprising computing a first predetermined function of power based on high voltage threshold (HVT) transistor gate area for high voltage threshold (HVT) devices and by computing a second predetermined function of power based on low voltage threshold (LVT) transistor gate area for low voltage threshold (LVT).

26. The method of claim 25, the estimating relative power by computing a predetermined characterization of power as a function of transistor gate area comprising estimating power by computing a third predetermined function of gate leakage power based on transistor gate area for both HVT devices and LVT devices.

27. The method of claim 25, the first predetermined function of power and the second predetermined function of power compute both static and dynamic power based on weights associated with both static and dynamic power.

28. The method of claim 23, further comprising repeating the calculating the transistor gate area associated with a circuit design and the estimating relative power by computing a predetermined characterization of power as a function of transistor gate area.

29. A computer-readable medium having computer-executable instructions for performing the method of claim 23.